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PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10038084	01/03/2002	~~257~~ 438	295	2814	A. D. MAI

**APPLICANTS: Falster Robert;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A DIV OF 09/737,715 12/15/2000 PAT 6,342,725
WHICH IS A CON OF 09/387,288 08/31/1999 PAT 6,236,104
WHICH CLAIMS BENEFIT OF 60/098,902 09/02/1998

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		MEMC 98-3052 (2512.2)
Verified and Acknowledged Examiners's intials			

TITLE : Silicon on insulator structure having a low defect density device layer and a process for the preparation thereof

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg. / Figs.Drwg.	Print Fig.
☐ TERMINAL DISCLAIMER		Primary Examiner	Applicati n Examiner	
		PREPARED FOR ISSUE		

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(Attached in pocket on right inside flap)